In the Claims:

1. (Currently Amended) A clocked cascadable power regulator, comprising:

synchronization logic that receives a clock signal and that asserts a digital output signal synchronized with said clock signal in response to assertion of a digital input signal; and

PWM control logic that controls each PWM cycle in response to said digital input signal and an output control condition; and wherein

said PWM control logic comprises

PWM logic that initiates a PWM cycle in response to said digital input signal and that terminates said PWM cycle in response to a reset signal; and

feedback sense logic, coupled to said PWM logic, that asserts said reset signal when said output control condition is met; and wherein

said PWM control logic comprises

a latch that sets in response to said digital input signal and that resets in response to said reset signal;

gate control logic, coupled to said latch, that provides at least one PWM activation signal; and

at least one driver amplifier, each responsive to said at least one PWM activation signal; and wherein

said feedback sense logic comprises

a sense amplifier that senses an output current condition and that asserts a sense signal; and

a comparator that compares said sense signal with a feedback reference signal to determine said output control condition.

2. - 4. (Canceled)

5. (Currently Amended) ~~The clocked cascadable power regulator of claim 1~~, A clocked cascadable power regulator, comprising:

synchronization logic that receives a clock signal and that asserts a digital output signal synchronized with said clock signal in response to assertion of a digital input signal; and

PWM control logic that controls each PWM cycle in response to said digital input signal and an output control condition; and further comprising

startup logic that disables synchronous cascaded operation during initialization.

6.(Currently Amended) ~~The clocked cascadable power regulator of claim 1,~~ A clocked cascadable power regulator, comprising:

synchronization logic that receives a clock signal and that asserts a digital output signal synchronized with said clock signal in response to assertion of a digital input signal; and

PWM control logic that controls each PWM cycle in response to said digital input signal and an output control condition; and wherein

said synchronization logic comprises cascaded flip-flops responsive to said clock signal and said digital input signal.

7. (Currently Amended) ~~The clocked cascadable power regulator of claim 1,~~ A clocked cascadable power regulator, comprising:

synchronization logic that receives a clock signal and that asserts a digital output signal synchronized with said clock signal in response to assertion of a digital input signal; and

PWM control logic that controls each PWM cycle in response to said digital input signal and an output control condition; and further comprising

a weak pull-down device coupled to pull-down said digital output signal unless otherwise driven high by a digital output signal from another regulator.

8. (Original) A multiphase power converter, comprising:

a plurality of regulators coupled in a cascade configuration, each comprising:

synchronization logic receiving a clock signal and a digital start input signal from a previous regulator and that provides a digital start output signal to a next regulator in response to said digital start input signal and synchronized with said clock signal; and

PWM control circuit that controls a PWM output in response to assertion of said digital start input signal and based on meeting an output condition;

a plurality of switching circuits, each having an input coupled to a PWM output of a corresponding one of said plurality of regulators, an output for driving a common DC output voltage, and a sense output provided to a PWM control circuit of said corresponding regulator; and

a controller that senses said DC output voltage and that provides a compensation signal to said PWM control circuit of said corresponding regulator and that provides said clock signal.

9. (Original) The multiphase power converter of claim 8, wherein said PWM control circuit comprises:

PWM logic that controls said PWM output based on assertion of said digital start input signal and a reset signal; and

feedback sense logic, coupled to said PWM logic, that asserts said reset signal based on said compensation signal and said sense output of a corresponding one of said plurality of switching circuits.

10. (Original) The multiphase power converter of claim 9, wherein said PWM logic comprises gate control logic and at least one driver amplifier.

11. (Original) The multiphase power converter of claim 9, wherein said feedback sense logic comprises:

a sense amplifier having an output and an input coupled to said sense output of said corresponding switching circuit; and

a comparator having a first input receiving said compensation signal, a second input coupled to said output of said sense amplifier, and an output that provides said reset signal.

12. (Original) The multiphase power converter of claim 8, wherein each of said plurality of switching circuits comprises:

first and second switches having current terminals coupled in series at a junction and having control inputs coupled to said PWM output of said corresponding regulator;

an output inductor coupled between said junction and said DC output voltage; and

a sense circuit that senses current of said output inductor and that provides said sense output.

13. (Original) The multiphase power converter of claim 8, wherein said controller comprises:

a sense amplifier having an input coupled to said DC output voltage and an output that provides an output sense signal;

an error amplifier that compares said output sense signal with a reference signal and that provides said compensation signal; and

a clock circuit that generates said clock signal.

14. (Original) The multiphase power converter of claim 8, wherein said plurality of regulators comprise N regulators coupled in a daisy-chain configuration, and wherein a selected switching frequency FSW is achieved by programming said clock signal with a frequency of N*FSW.

15. (Original) The multiphase power converter of claim 8, further comprising a pull-up device coupled to initially pull high a digital start input signal of a first of said plurality of regulators.

16. - 20. (Canceled)